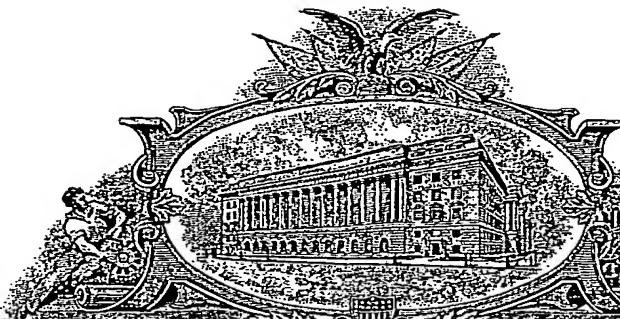


10/519331

22 DEC 2004



REC'D 01 AUG 2003  
WIPO PCT

PI 1044250

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office

July 25, 2003

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM  
THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK  
OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT  
APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A  
FILING DATE.

APPLICATION NUMBER: 60/396,743 -

FILING DATE: *July 19, 2002*

RELATED PCT APPLICATION NUMBER: *PCT/US03/19984*

By Authority of the  
COMMISSIONER OF PATENTS AND TRADEMARKS



  
H. L. JACKSON  
Certifying Officer

**PRIORITY  
DOCUMENT**

SUBMITTED OR TRANSMITTED IN  
COMPLIANCE WITH RULE 17.1(a) OR (b)

601346743 - 07192002  
R10Rou

Please type a plus sign (+) inside this box →

Approved for use through 10/31/2002 OMB 0651-0032

U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE  
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**PROVISIONAL APPLICATION FOR PATENT COVER SHEET**  
This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

20/67/02

PTO

34162

7/19/02

INVENTOR(S)		
<input type="checkbox"/> Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Yoshihide Sang-In	SENZAKI LEE	Aptos, California Scotts Valley, California
<input type="checkbox"/> Additional inventors are being named on the _____ separately numbered sheets attached hereto		
TITLE OF THE INVENTION (280 characters max)		
Vacuum UV Assisted Atomic Layer Deposition		
Direct all correspondence to: CORRESPONDENCE ADDRESS		
<input type="checkbox"/> Customer Number	<input type="text"/> →	
OR <input type="text"/> Place Customer Number Bar Code Label here		
<input checked="" type="checkbox"/> Firm or Individual Name	Dorsey & Whitney LLP	
Address	850 Hansen Way, Suite 200	
Address		
City	Palo Alto	State California ZIP 94304-1017
Country	USA	Telephone 650-494-8700 Fax 650-494-8771
ENCLOSED APPLICATION PARTS (check all that apply)		
<input checked="" type="checkbox"/> Specification Number of Pages	6	<input type="checkbox"/> CD(s), Number <input type="text"/>
<input type="checkbox"/> Drawing(s) Number of Sheets <input type="text"/>		<input type="checkbox"/> Other (specify) <input type="text"/>
<input type="checkbox"/> Application Data Sheet. See 37 CFR 1.76		
METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)		
<input type="checkbox"/> A check or money order is enclosed to cover the filing fees	FILING FEE AMOUNT (\$)	
<input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number <input type="text" value="50-2319"/>	\$160.00	
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.		
The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.		
<input type="checkbox"/> No.		
<input type="checkbox"/> Yes, the name of the U.S. Government agency and the Government contract number are <input type="text"/>		

Respectfully submitted,

SIGNATURE

*Daniel E. Fisher*

Date 7/19/2

TYPED or PRINTED NAME Daniel E. Fisher

REGISTRATION NO.  
(if appropriate)

34,162

TELEPHONE 202-442-3000 or 650-494-8700

Docket Number:

71642

**USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT**

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C.

P19LARGE/REV05

## VACUUM UV ASSISTED ATOMIC LAYER DEPOSITION

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The present invention relates generally to the field of semiconductors. More 5 specifically, the present invention relates to atomic layer deposition on semiconductor devices and wafers.

#### Description Of Related Art

Semiconductor devices of future generation require thinner dielectric films for 10 MOS transistor gates, and capacitor dielectrics. As oxides are scaled down, the tunneling leakage current becomes significant and limits the useful range for gate oxides to about 1.8 nm or more.

High dielectric constant metal oxides such as  $\text{HfO}_2$  ( $k=20\sim 25$ ),  $\text{ZrO}_2$  ( $k=20\sim 25$ ) and Hf and Zr silicates are considered alternative materials to silicon oxide ( $k=3.9$ ) to 15 provide gate dielectrics with high capacitance without compromising the leakage current. However, prior art deposition techniques such as chemical vapor deposition (CVD) are increasingly unable to meet the requirements of advanced thin films. While CVD processes can be tailored to provide conformal films with improved step coverage, CVD processes often require high processing temperatures, result in incorporation of high 20 impurity concentrations, and have poor precursor or reactant utilization efficiency. For instance, one of the obstacles of making high  $k$  gate dielectrics is the formation of an interfacial silicon oxide layer during CVD processes. Another obstacle is the limitation of

prior art CVD processes in depositing ultra thin films for high k gate dielectrics on a silicon substrate.

Atomic layer deposition (ALD) is an alternative to traditional CVD processes to deposit very thin films. ALD has several advantages over traditional CVD. ALD can

5 produce conformal thin film layers on non-planar substrates. More advantageously, ALD can control film thickness on an atomic scale, and can be used to "nano-engineer" complex thin films. ALD can also be performed at comparatively lower temperatures which is compatible with the industry's trend toward lower temperatures. Once such technique is described by A. Schurmann in U.S. Patent No. 5,916,365, titled "Sequential Chemical  
10 Vapor Deposition." However, even at these relatively lower temperatures, oxygen from a metal oxide layer diffuses into Si substrates and forms a  $\text{SiO}_x$  sub oxide layer at the interface between gate or capacitor dielectric and the substrate, and degrades the gate stack integration. Accordingly, further developments in ALD are highly desirable.

Since late 90's, numerous papers have been reported on the interfacial oxide growth problem for gate and capacitor dielectric applications. This problem is one of the 15 major hurdle for implementing high-k materials in advanced device fabrication.

A Xe excimer lamp was utilized by Kurosawa et al. for a room temperature photolitic CVD of  $\text{SiO}_2$  from tetraethoxyorthosilicate (TEOS) on single crystalline  $\text{Al}_2\text{O}_3$  substrate. A schematic drawing of the reactor shown below is cited from the literature (Appl Phys. Lett., 20 vol.69, p.1399 (1996)) and is hereby incorporated by reference. A method for a room, or near room, temperature ALD would be advantageous by providing the benefits of ALD without the drawbacks of interfacial oxide growth.

25

#### SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method and system of forming films on semiconductor devices and wafers by atomic layer deposition at or near room temperature.

30 These and other objects are achieved by the present method and system where a substrate having a film deposited on the surface of the substrate in a vacuum UV (VUV)

assisted atomic layer deposition process. A reactant gas or set of gasses is introduced into a vacuum chamber to react with a first layer of the film to convert the first layer into a mono-layer of a solid compound. Optionally, an oxidant gas is introduced in combination with reactant gas. Excess reactant gas is then purged from the chamber. The surface of the 5 substrate is subjected to VUV radiation. Excess gas is again purged from the chamber. The cycle is repeated as necessary using the same or different reactant gases.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention provides a novel atomic layer deposition method and system.

10 When referring to the deposition aspect of the method, the abbreviation ALD is often used. In general the present invention provides an ALD method and system where a film is deposited on a substrate at room, or near room, temperature, often referred to as ambient temperature. The deposition is accomplished with the assistance of vacuum ultra-violet radiation (VUV). Generally, the steps of the method consist of placing a substrate into a 15 vacuum chamber. Introducing a reactant gas, or combination of gasses, into the chamber to react with the substrate (a silicon surface or a layer of the ALD film) to convert the layer into a mono-layer of a solid compound. Then the excess reactant gas or gasses are purged from the chamber. Then the chamber is evacuated of gases and the mono-layer on the substrate is irradiated with UV radiation. Re-purging the excess gas from the chamber, 20 and repeating the cycle as necessary completes the process.

One application of the present invention provides for the deposition of a high dielectric constant (high-k) metal oxides onto a silicon substrate. Of particular advantage to this application is that the deposition is performed at lower temperatures thereby suppressing the formation of interfacial oxide growth between dielectric and silicon 25 surface. The method of the present invention can be performed at a temperature in the range of about ambient to 200°C, preferably at ambient temperature.

For example, oxygen containing metal-organic complex, such as Hf(t-BuO)<sub>4</sub>, Zr(t-BuO)<sub>4</sub> etc., can be used as precursors for depositing HfO<sub>2</sub> and ZrO<sub>2</sub> onto a silicon 30 substrate. The reaction can optionally include oxidant gases and proceeds at low temperature using the VUV-assisted ALD process of the present invention.

More specifically, in one aspect of the present invention, a method of depositing a thin dielectric film on a substrate using VUV assisted ALD is provided. According to the present method, a substrate, such as a silicon wafer, on which a film is to be deposited, is placed in a reactor. The substrate can be of any type including a film deposited on a 5 substrate as used in semiconductor processing such as any gate dielectric or ceramic, including metal oxides, aluminates, silicates, nitrides, or pure metals.

The reactor is a vacuum chamber equipped such that VUV radiation can be introduced into the chamber. The chamber must also be set up so that reactant gasses can be introduced and purged from the chamber. An example of such a set up is disclosed by 10 Kurosawa et al as discussed in background section of this application. A Xe excimer lamp can be used as a source of the VUV radiation. The Xe excimer lamp can be used for a large area irradiation, and therefore, it is a suitable energy source for photo-assisted ALD of ultrathin high-k gate dielectrics at a low deposition temperature. Other UV sources, however, also can be used for large area irradiation, and therefore, may also be acceptable. The Xe excimer 15 lamp irradiates at a wavelength of 172 nm. Different types of lamps provide different wavelengths and correspondingly will deliver different photon energies. Irradiation at other wavelengths under 200 nm may be desirable depending on the particular application and the amount of photon energy required.

A reactant gas is introduced into the reactor to react with the substrate or a surface 20 layer of film to convert the layer into a mono-layer of a solid compound. The excessive reactant gas is evacuated from the reactor with an inert purge gas. Optionally, an oxidant gas can be introduced into the reactor. The chamber is not irradiated as these steps are performed; either the lamp is off or the lamp is on with the shutter closed.

Thereafter, the lamp is turned on and the shutter is opened irradiating the chamber 25 and the surface of the substrate. The duration of the irradiation is about 0.1 seconds to 10 seconds. The vacuum strength is in the range of about 10 torr down to  $1 \times 10^{-8}$  torr. After irradiation, the chamber is again purged to evacuate any excess reactant gas. This cycle can be repeated as necessary with the same reactant gasses or different ones, depending on the application. Typically, the cycle is repeated 10 to several hundred times. During 30 subsequent cycles the duration of the irradiation, the wavelength of the irradiation, and the

60396743 .07.1902

strength of the vacuum can all be varied according to the needs of the specific application. The selection of the these variables depend on the nature of the reactant gases and the chemical bonds involved in the deposition.

Having thus described the invention with the details and particularity required by

5 the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

What is claimed is:

1. A method for depositing an atomic layer on a substrate comprising:
  - (a) placing a substrate into a vacuum chamber;
  - (b) introducing reactant gas or gasses into the vacuum chamber;
  - (c) purging any excess reactant gas from the vacuum chamber;
  - (d) irradiating the surface of the substrate with vacuum ultra-violet radiation;
  - (e) re-purging the chamber; and,
  - (f) repeating steps (a) through (e) a plurality of times with the same or different reactant gasses.
2. The method of claim 1 further comprising introducing an oxidant into the chamber after step (c) and prior to step (d).